New PIO stuff which I may or may not have understood: totally untested

In theory the following assembler statements are now supported

mov rxfifo[y], isr mov rxfifo[<index>], isr mov osr, rxfifo[y] mov osr, rxfifo[<index>]

In addition two new parameters to the shiftctlr function

push threshold,pull threshold,[autopush],[autopull],[IN\_SHIFTDIR],[OUT\_SHIFTDIR],[FJOIN\_RX],[FJOIN\_TX],[FJOIN\_RX\_GET,[FJ OIN\_RX\_PUT

Then a new subcommand

WRITEFIFO pio, sm, fifo, value

and a new function

PIO(READFIFO pio, sm, fifo)

If I understand correctly, you need to enable either FJOIN\_RX\_GET, and/or FJOIN\_RX\_PUT in order for the new assembler statements to do anything and then, depending on them being enabled you can read and/or write directly to the FIFO cells

Quote When only SHIFTCTRL\_FJOIN\_RX\_PUT is set (in SM0\_SHIFTCTRL through SM3\_SHIFTCTRL), the system can also read the RX

FIFO registers with random access via RXF0\_PUTGET0 through RXF0\_PUTGET3 (where RXFx indicates which state

machine’s FIFO is being accessed). In this state, the FIFO register storage is repurposed as status registers, which the

state machine can update at any time and the system can read at any time. For example, a quadrature decoder program

could maintain the current step count in a status register at all times, rather than pushing to the RX FIFO and potentially

blocking.

Quote When only SHIFTCTRL\_FJOIN\_RX\_GET is set, the system can also write the RX FIFO registers with random access via

RXF0\_PUTGET0 through RXF0\_PUTGET3 (where RXFx indicates which state machine’s FIFO is being accessed). In this

state, the RX FIFO register storage is repurposed as additional configuration registers, which the system can update at

any time and the state machine can read at any time. For example, a UART TX program might use these registers to

configure the number of data bits, or the presence of an additional stop bit.

Quote When both SHIFTCTRL\_FJOIN\_RX\_PUT and SHIFTCTRL\_FJOIN\_RX\_GET are set, the system can no longer access the RX FIFO

storage registers, but the state machine can now put/get the registers in arbitrary

order, allowing them to be used as additional scratch storage.

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